

ATM PACKET SWITCHING FOR AIRBORNE/SPACE PAYLOADS

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ABSTRACT

Systems & Processes Engineering Corporation (SPEC) under contract with the Air Force's Rome Laboratory has designed, built, and tested a 9 x 9 prototype Fast Packet Satellite Switch (FPSS) which has basic Asynchronous Transfer Mode (ATM) packet compatibility and a port speed of 155 Mbps. An operational FPSS will ultimately support multiplexed high-speed traffic which is transmitted from a DoD gateway, demultiplexed on-board a satellite, and downlinked to individual tactical users on a packet by packet basis. FPSS provides multiple connectivity among military users through satellite virtual packets (SVPs), which enclose and transport ATM packets. ATM compatibility minimizes delay and wasted capacity for channel allocation, and utilizes a minimum of space segment resources with its inherent bandwidth-on-demand characteristics. The next phase of this program will be aimed at reducing the digital circuit power requirements for future military airborne/space payloads.

INTRODUCTION

Early communication satellites, and many still in service, have a simple transponder architecture – each transmitter on the satellite is permanently wired to one receiver. The early satellite transmitter antennas had relatively wide coverage of the earth below, and there were no crosslinks to other satellites. Later, with more directional antennas, satellites such as INMARSAT III included connection switching circuits to allow a receiver to be connected to any of several transmitters each aimed at a distinct spot on the earth's surface; however the control of these connection switches remained on the ground at a master site. Connection setup protocols are sluggish because the user must contact the master site for clearance and then the master site must configure the satellite.

An improvement was obtained for the INTELSAT VI satellites by switching each receiver to all of the transmitters in a regular cycle. By gating uplink transmissions to the proper time slice a single uplink could select any of the downlinks, which also

simplifies earth station design. However, it is still necessary to allocate channel use from a master ground site to avoid signal overlap between user signals, and for billing. The next step is to move routine channel allocation to the satellite while metering use and retaining high level control.

Does that mean that the DoD needs satellites with on board switching? The answer is most definitely yes! Lessons learned from Desert Storm show that the lack of high speed communications for imagery dissemination, logistics, personnel, and medical was a real problem.¹ Both military and commercial communications channels became clogged because of low rate of circuits and because of inefficient routing and forwarding procedures.

With the success of packet switched data communication and the general trend to digitization of analog signals, communication switching hardware is shifting away from traditional circuit switches and toward packet switches. The packet switch hardware picks out the destination of each packet from its header and routes the packet to an output, bypassing the more complex process of circuit setup from end to end. Asynchronous Transfer Mode (ATM) is, at its lowest level a very high speed packet switch; however it is much more complex than that because it includes hardware and protocols to set up and tear down virtual circuits (simulated by packet streams) with demand-driven bandwidth allocation. Longer term it appears that ATM will dominate the high speed commercial networks.

ATM has been embraced by the DoD as the communications mode of choice for modern high-speed imagery dissemination, file transfer, and teleconferencing. Why not use ATM as the architecture for a satellite communications switch? There are several reasons. ATM standards for terrestrial systems have yet to be finalized. Since satellites are designed for long lifetime (15 years for a geosynchronous satellite, for example) satellite developers are unwilling to adopt a technology that can change format over the next few years. ATM is a complex protocol with complex equipment; this in

itself is worrisome for a satellite where repair is expensive or impossible. ATM was designed for the relatively noise free communication media of fiber optics and it may need modification for space.

FPSS is a natural intermediate step toward developing a full ATM switch. A FPSS can be designed with a simplified protocol to transport ATM packets between terrestrial ATM switches. The same FPSS can be used to support the emerging packet-based tactical systems to enhance the DoD's communications capability in the near future. Adoption of ATM-compatible FPSS in the military communications system will not only make it more adapted to its ongoing standardization program but also provide flexible, real-time bandwidth allocation and simpler payload control.

To use the FPSS with ATM, an earthside hardware interface is required to perform a simple translation from ATM cells to/from Satellite Virtual Packets (SVPs). The SVP is a few bytes larger than the standard 53-byte ATM cell (packet) to accommodate a header for routing through the satellite. Other traffic with different packet sizes will be translated by a similar hardware interface.

With the faster space-qualified integrated circuit (IC) technologies becoming available, we can design faster (higher data rate) packet switches with more sophisticated functions to support data, voice, video, and eventually a full ATM switch.

Rome Laboratory funded this research effort in October of 1995 with the goal of developing a prototype FPSS around a 9 x 9 crossbar architecture with a 155 Mbps per port speed. The original plan was to fly this prototype on a low cost test satellite with later implementation onto a MILSTAR or DCSC satellite. SPEC and Rome Laboratory are also looking to use this prototype in similar environments which require the FPSS's capabilities. One potential environment is on Unmanned Aerial Vehicles carrying communications payloads. The FPSS would allow multiple traffic streams to be sent simultaneously. These links could be set up independently and would not require previous ground configuration set-up. SPECS is also in negotiations with two major corporations over use of these ASIC designs.

SATELLITE VIRTUAL PACKET FOR FPSS

The satellite virtual packet (SVP) format for the 9 X 9 FPSS prototype is shown in Figure 1. The SVP consists of one priority bit, two nine bit routing tags, a five bit Header Error Correction (HEC) code, and 424 bits (53 bytes) of payload data. Error correction of the payload data was not included because would have

added too many bits. The header represents a tradeoff between flexibility and bit overhead. Routing tag #1 is the minimum necessary header information and indicates which output to route the SVP. Routing tag #2 may be used to select earth stations located within a downlink beam or it may be used by another FPSS located in a second satellite crosslinked to the first. The routing tags are not encoded so as to support multicast and broadcast. Figure 2 displays an example routing tag where the signal is being "multi-casted" to outputs 1 and 5.

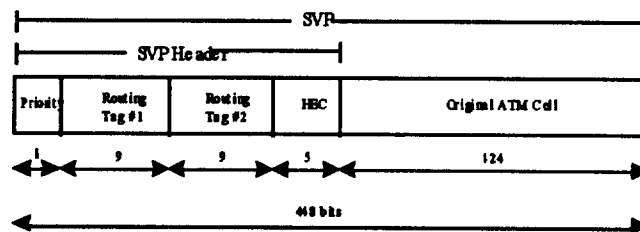


Figure 1. SVP Format

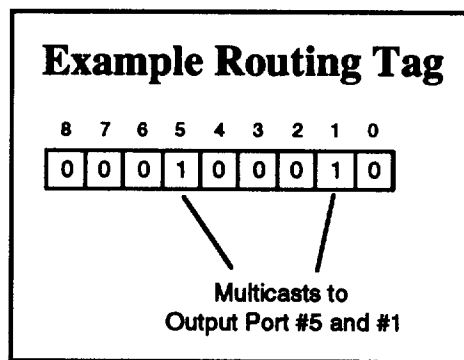


Figure 2. Example Routing Tag

FPSS HARDWARE DESIGN

The FPSS design is a packet switch which allows eight independent input packet streams to feed eight independent output packet streams and performs the necessary routing of packets as they are transported across the switch. Each input packet stream is taken from an uplink receiver and each output packet stream goes to a downlink transmitter, as shown in Figure 3. The FPSS includes nine input processors, nine output processors, a central crossbar and contention/congestion control circuits, and an interface to an On-Board Network Controller (OBNC). Each I/O processor has packet buffer memory (not shown in Figure 3) enough to hold 256 packets. The ninth output processor is connected back to the OBNC so that the OBNC can receive packets from the ground

stations. The ninth input processor is connected to the OBNC so that the OBNC can send packets to the ground stations.

Since the packets are routed from uplink to downlink beams according to the packet header information, the FPSS control is "connectionless" (packet switched as opposed to circuit switched). Note that since packets from more than one input can be routed to a single output, packets can accumulate in an output buffer faster than they can be transmitted away. Therefore the FPSS requires flow and congestion control to minimize packet loss at the satellite.

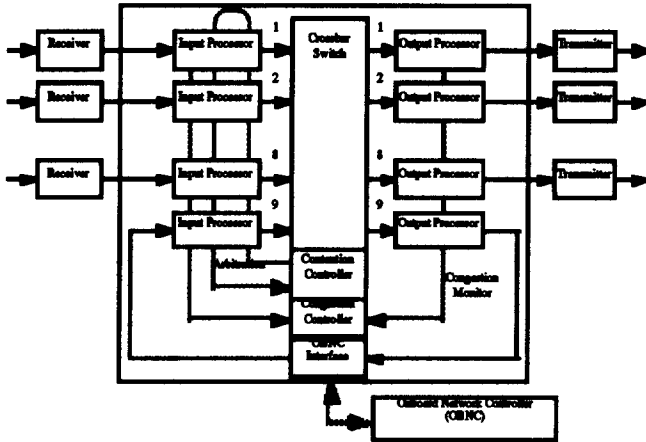


Figure 3. 9 x 9 Crossbar Switch

The heart of the FPSS is the 9 X 9 crossbar switch, which is implemented with multiplexers. Packets are transported across the switch serially, one bit per clock. To prevent the crossbar from becoming the bottleneck in the system, the data rate through it on a single wire is designed to be at least 330 Mbps, or twice the rate of an uplink port (155 Mbps). The 9 X 9 crossbar and its related control and interface circuits of Figure 3 are realized on one GaAs ASIC. The block diagram for this "crossbar ASIC" is shown in Figure 4.

The crossbar ASIC routes packets from the input processors to the output processors. It also manages the congestion control (contention detection and arbitration) and communicates with the OBNC. As shown in Figure 4, the crossbar matrix receives input signals from the nine IPs and routing control signals from the contention controller. With this information, the crossbar matrix is able to send the packets to the corresponding nine OPs. The contention controller in turn receives routing tags from the IPs and OBNC and uses this information to formulate the routing control signals. IP#9 and OP#9 communicate with the OBNC through the OBNC interface and the buffer controllers.

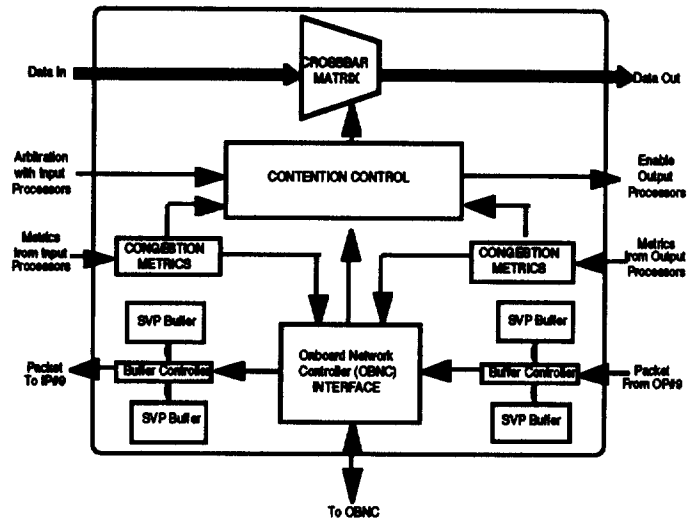


Figure 4. Block Diagram

The input processor (IP) has four major functions. First, it reads data from receiver. It stores packets in SRAM buffer and corrects errors on readout. It participates in contention control and arbitration. Finally, it tracks congestion and buffer usage. The IP is realized in one GaAs ASIC and two CMOS SRAMs.

The output processor (OP) performs essentially the same functions as the input processor, except that its input is the higher speed side instead of its output. It too is realized in one GaAs ASIC and two CMOS SRAMs.

Each SRAM buffer is organized as 32K words x 16 bits/word and its structure is displayed in Figure 5. The stored SVPs are organized into a doubly linked-list in order to facilitate adding to, scanning through, and removing packets from the buffers. The buffer size was chosen to hold 256 packets to minimize control logic while maintaining enough size to minimize dropped (lost) packets.^d

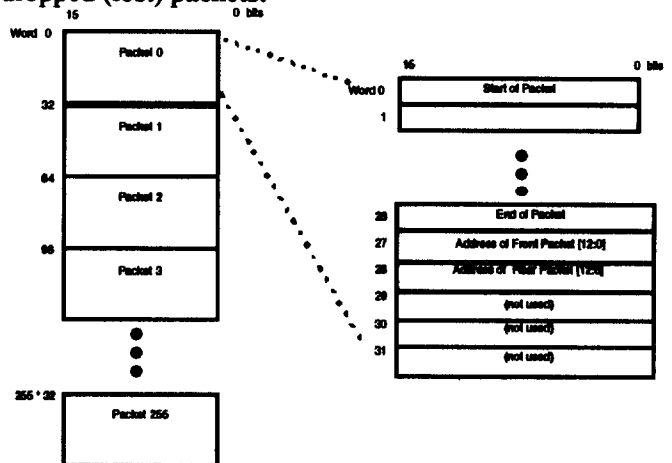


Figure 5. SRAM Structure

All input buffers are given equal opportunity to send a packet through the crossbar by a scan from the congestion with rotating starting position. Buffer free space for the IPs and OPs are continuously monitored by the OBNC to avoid congestion. When buffers begin to fill up, the OBNC generates packets to signal the related Earth stations to throttle-back their uplinks. If the uplink cannot slow down quickly enough, then the buffers may overflow and some packets will be discarded (lost). Packet discard is governed by packet priority.

The current FPSS design has two levels of priority. These levels are indicated by the header bit. The highest priority packets will reserve output slots first and the lowest priority packets will be discarded first.

ERROR CORRECTION

Certain portions of the FPSS are more sensitive to bit errors due to space radiation and thermal noise than others. Because a packet sent to the wrong address wastes downlink time immediately, the routing tags are protected by the Header Error Correction code. For persistent data, a number of critical control registers are protected by using a majority logic scrubbing technique. This utilizes three redundant registers for each bit value and regularly compares the values held in those three registers to determine the bit value used. If any register disagrees with the other two, it is re-written to match the majority value. In addition, distance three Hamming encoders/decoders are used to insure that the SRAMs' linked lists are kept intact. Since the payload data dwell time on the satellite is small we do not error correct it. In some cases it would be redundant to error correct the payload due to internal error correction.

The final design consideration which had to be addressed was the area of radiation hardening for space application. GaAs ICs have excellent total dose radiation immunity, about 100 times better than CMOS, but they have shown poor soft error upset (SEU) immunity. A new low temperature buffer treatment appears to provide excellent SEU immunity & low leakage current.²

PROTOTYPE TESTING

We have included boundary scan circuits (JTAG compatible) on the GaAs chips to test the individual chips and the prototype FPSS assembly on a card. Through a JTAG serial test port, the state of each chip I/Os can be set or scanned out. In this way we verify the operation of each chip and the connections between chips on a card. The FPSS prototype is a card with

one crossbar chip, nine input processors, nine output processors, and 36 fast SRAMs.

In order to test the FPSS, the configuration in Figure 6 is employed. A fast pattern generator is used to simulate the input packet serial streams which are sent to the FPSS prototype card via ribbon cable. The FPSS creates the output packet serial streams which are sent to a fast logic analyzer via ribbon cable. The PC test controller is linked to the generator and analyzer via IEEE 488 bus. The PC test controller programs the generator for a specific set of packets with specific destinations. The output packets are captured by the logic analyzer and sent to the PC test controller for comparison to the expected pattern. Theoretically no direct connection is needed between the OBNC and the PC but, one is provided to escape from unrecoverable faults if needed.

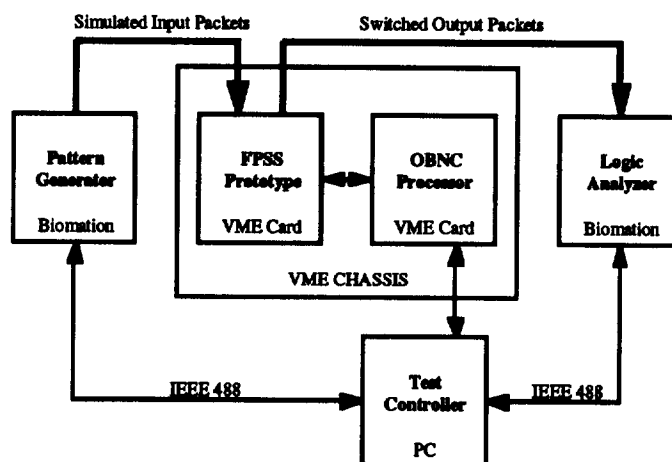


Figure 6. Test Configuration

CONCLUSIONS

The FPSS has the potential to provide the military and commercial sectors a connectionless satellite switching mechanism to support numerous military facilities in the theater, provide bandwidth on demand to the subscribers, and amortize the expensive satellite resource by sharing the satellite switch payload. In simple terms, FPSS paves the way to placing an ATM switch in the sky.

This current design used Vitesse E/D MESFET technology which has excellent performance in the 500 MHz to 2 GHz range, multiple logic families, medium to high power, medium cost, integration levels on the order to 300K gates or higher, and standard cell libraries available. The next phase of this work for military applications will be to produce a FPSS using Honeywell/Motorola's CHFET technology. The most significant characteristic of this technology is its

extremely low power consumption, which is one-sixth that of CMOS, primarily due to much lower supply voltage. SPEC began developing standard cell libraries for CHFET in early 1996 in preparation for this next phase.

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REFERENCES

1. Personal communication from Dr. N. Bernie Penrose at SPEC.
2. Todd Weatherford, et. al., "Soft Error Immune LT GaAs ICs," IEEE GaAs IC Symposium, Orlando FL, Nov 1996.
3. Yasuro Shobatake, *et al.*, "A One-Chip Scalable 8*8 ATM Switch LSI Employing Shared Buffer Architecture," in *IEEE Journal on Selected Areas in Communication*, vol. 9, no. 8, Oct. 1991, pp. 1249-1253.